AimValley

Project Example
Ultra Low Latency

Customer
A supplier of industrial equipment needs a replacement for their system control infrastructure. Their current solution is based on legacy technology and protocols, and component availability becomes a serious concern going forward.

Customer Objectives
Development of a future proof architecture and design of building blocks for the control plane with a focus on ultra low latency. The target for end-to-end latency across the infrastructure is in the sub-micro second range.

Customer Benefits
Our solution supports both the current systems and the next generation architecture. This allows the customer to support continued supply and manufacturing of equipment, mitigating their concerns about component obsolescence. And to use the same architecture for the future systems, preventing the need for multiple parallel developments, and high amount of reuse for software, tools and factory test configurations.

AimValley Solution
The project is delivered in multiple stages, starting with a study phase where we do detailed analysis of all relevant requirements and parameters contributing to latency. This includes investigation of available technologies, compatibility with existing infrastructure and modeling various solutions, using simulation and lab validation. We selected an FPGA-based solution as best fitting with the objectives of the customer.

Key Technologies
- Consultancy on connectivity protocols by Systems Engineering team.
- Expertise on high-speed serial interfaces and serial/parallel conversion delays in FPGAs.
- Modeling and simulations of data delays in FPGAs.
- Implementation and validation measurements of sub-micro second latency on FPGAs.

Results and Added Value

Efficient
A flexible solution is delivered supporting current and future equipment generations, based on a single and re-usable FPGA design.

Successful
The customer had found standard IP solutions with a poor latency performance, in the order of several micro seconds. With our solution, an end-to-end latency far below micro second is achieved.

Partnership
AimValley teams work closely with system architects of the customer to define required performance.

Innovation
Ultra low latency is achieved by exploiting specific functionality of the FPGA SerDes and focus on efficient transfer of data across the chip.

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