



### Solving design challenges for the Terabit era!

The volume of traffic being transported on the world's telecom networks has been rising exponentially for decades. In recent years streaming video has, by far, become the largest portion of the traffic and overall traffic is now almost exclusively Ethernet packets, with video, voice, data, and machine to machine communication being encoded into packet streams. In terms of the physical build-out of telecom networks, fiber optic cable is used for the vast majority of long haul transport and it is also used in metropolitan networks, cell tower connections, corporate enterprise networks, and more and more is becoming the physical media to connect homes.

To accommodate the ever-rising amount of transported data, communication and internet service providers have continuously added additional fiber.

Equally important is that technology has continued to evolve such that transmission rates have increased in several orders of magnitudes. The key advantage provided through upgrades of transport gear that carry far higher bit rates, is the elimination of the need to install new fibers. That is especially important in long and medium haul fiber routes where the physical construction work across long distance routes is both expensive and time consuming.

The predominant transport technology is Ethernet over optical transport using Dense Wavelength Division Multiplexing (DWDM). Optical Transport Network (OTN) mapping provides additional quality and eases operational maintenance for telecom operators. Common optical transport data rates are 100, 400, 800 Gb/s and soon networks will enter the Tb/s era.

## Challenges at the physical layer

As data rates increase it becomes harder to mitigate transmission impairments due to noise, attenuation, amplitude or phase errors, and optical dispersion.

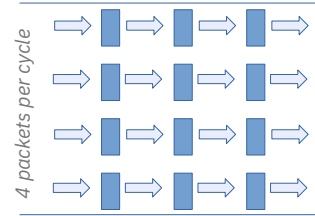
Let's review some of the most important measures and techniques that can be applied to achieve reliable connections at higher data rates:

- Line coding and higher order modulations map binary data bits to analog signals on the physical media. There are many aspects to be considered when selecting a specific code and modulation scheme, e.g.: medium characteristics, spectral density, channel interference, noise tolerance, and demodulation algorithm complexity.
- Forward Error Correction (FEC) enables the detection and correction of bit errors caused by various physical impairments in the transmission medium, for example: attenuation, noise, dispersion or cross-talk.
- Optical Coherent Transmission: helped by major advances in silicon technology, such as 5 nm CMOS, it is now possible to handle coherent transmission in a compact optical module form factor. These highly programmable modules support a multitude of modulation formats, OTN mapping, error correction and various means to combat optical impairments such as attenuation and various types of dispersion.

## Terabit Packet Processing in FPGA

As data rates on optical interfaces increase, also switching nodes need to cope with the higher packet forwarding speed. On a Terabit Ethernet link short data packets arrive at a rate of about 1.4 GHz, which is higher than the internal clock rate of high-end FPGAs. As a result, a Terabit processor requires very wide internal data paths, e.g. 2048 bits at 0.5 GHz clock.

Furthermore, the packet processing pipeline needs to be able to handle multiple short packets in parallel.



Productivity tools such as HLS and P4 help to deliver such complex designs with high flexibility and meeting the required quality in a shorter time-to-market.

## AimValley High Speed Ethernet Expertise

- Development of 100, 400 and 800G Ethernet interface cards for test equipment
- 100G Ethernet packet switch design
- Experts in high speed FPGA transceiver design
- FPGA based high data rate packet processing
- High bitrate hardware board designs achieving the required signal integrity with sufficient margin using analog and 3D simulation technology
- Development of Optical Transport Network (OTN) multiplex systems
- Architecture and design of clock and synchronization solutions at network, system, board or device level, including CDR, PLL and gearbox designs
- Architecture and design of Ultra Low Latency switch

### AimValley proven track record

- [800G Gearbox Mezzanine Board](#)
- [400G FPGA PCIe Card](#)
- [400G-800G Transmission](#)
- [Ultra Low Latency](#)

## Why AimValley?

AimValley is a reliable provider of ultra high speed Ethernet backhaul technology since 2003, delivering solutions for:

- High speed data processing applications
- Complex FPGA-based accelerated systems
- High speed, low power hardware equipment
- Robust embedded software
- Early adopter of Acceleration Technology

AimValley understands the full complexities as well as the subtle nuances of designing great edge solutions. We excel in building complex systems that are part of your product in the fields of

Telecom, Industry 4.0, Healthcare and Transportation markets. Our combined skills represent all the important aspects required for the development of end-to-end systems.

Our customers enjoy the benefits of working with a strong team with over 2000 years engineering experience. AimValley is a trusted partner of Tier 1 customers in Telecom and Industrial markets and has shipped more than 100 000 products.

## Quality Focus

- Outstanding track record of on-time delivery
- Best in Class Designs – Time, Budget & Quality
- ISO9001, ISO140001, EcoVadis Platinum CSR