AimValley

Project Example
FPGA Interposer

Customer
External events can have a sudden impact on product supply. A major earthquake and tsunami flooded a semiconductor manufacturing site and immediately affected delivery of silicon devices. One of the impacted devices was a custom ASIC designed for a series of telecom products. The Tier 1 Telecom Network Equipment Manufacturer was looking for an immediate replacement of the device that could otherwise halt system deliveries for a long period. They asked AimValley for a solution.

Customer Objectives
Customer needs a fast turn around time and cannot afford to wait for a full ASIC redesign cycle. Also the solution should not result in extra R&D effort for their internal system software or hardware design teams of the multiple affected product series.

Customer Benefits
By replacing an End-of-Life (EoL) device by an FPGA, AimValley is able to extend the life-cycle of the product. An FPGA design was chosen to reduce the time to market and resulting in short interruption in product supply.

AimValley Solution
AimValley developed a drop-in replacement based on an FPGA on an interposer design. The interposer is a small Printed Circuit Board that has the same footprint as the replaced ASIC. On the interposer board an FPGA performs the functionality of the replaced ASIC. Additional circuitry was added to handle multiple supply voltages and IO signaling differences between the ASIC and the interposer design.

Key Technologies
> FPGA design using regmap designer for 100% software compatibility.
> Hardware design with signal integrity simulation.

Design Briefs
> End-of-Life Chips

Results and Added Value

Efficient
The interposer-based design was completed in a much shorter interval than a full customer ASIC redo.

Successful
The design team worked closely with the customer's R&D hardware and software teams to ensure full compatibility of the interposer and FPGA-based solution.

Partnership
The design is fully Hardware compatible with the existing system boards and could be used as a drop-in replacement. It was also 100% Software compatible with the ASIC, preventing rewrite of code and no need for a full SVT cycle. As a result there was just a short interruption in system supply to customers.

Innovation
The FPGA lacked the technology specific LVDS IO signaling type of the ASIC. An alternative was found by emulating the required signaling with additional circuitry on the interposer board, effectively resulting in Hardware backward compatibility.

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