AimValley

# Student Assignment

## SoC Streaming Interface


AimValley is a world-class engineering and innovation center that designs and builds networking solutions. We are based in Hilversum, with colleagues in Canada, India and France. We started in 2003 as a spin-off from Lucent Technologies (a successor from the American company AT&T), which is why we have a strong background in telecommunication solutions and have built-up a vast expertise in real-time processor technology. Our telecom experience creates a perfect crossover to the HealthTech sector, where we are establishing our footprint, through developing innovative connectivity solutions for medical device manufacturers. Most of our design & development is done in-house.

Product development entails the preparation of requirements documents, specifications of system architecture, electronic development (board design, system certification, mechanical design), FPGA/ASIC & software development, system verification, and product/factory introduction. AimValley uses FPGAs to process high-speed transmission functions. Real-time requirements are key in our software development.

Our business is about people and our teams are dynamic, skilled and passionate about technology. Recruiting and training the right talent is an essential part of the AimValley DNA. We have over 95 employees of which 75% work as a design expert in the R&D organization. All R&D employees have a college or university-level education.

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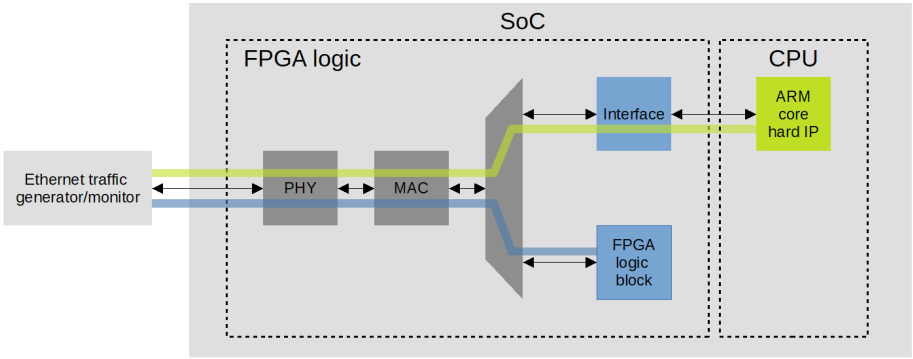
## SoC Streaming Interface

### Project Introduction - SoC Streaming Interface

AimValley has a long experience in system development, where FPGA's and processors are used in a product. However there is no experience with using a System on Chip (SoC), where an FPGA is combined with a hard core CPU on the same die. For certain projects it could be beneficial to have a SoC where the CPU can communicate directly to the FPGA logic and does not need a dedicated CPU interface like SPI or PCIe. AimValley wants to gain experience in using a streaming kind of interface like AXI to directly communicate with the on die processor.




### Project Description

Make an test design in the FPGA logic of a SoC as shown above

- The PHY and MAC will process the Ethernet Packets.
- The MUX will filter out 2 streams by a unique identifier and send one stream (green) to the ARM core and one stream (blue) to a FPGA logic block. and vice versa.
- The FPGA logic block will loop the Ethernet traffic and perform a simple but unique modification for identification.
- The ARM core will loop the Ethernet traffic and perform a simple but unique modification for identification.
- The interface will handle the streaming traffic to and from the ARM core.

Develop and document the interface between the FPGA logic and the ARM core. This is the most important part for AimValley. It is recommended to have focus on this part.
Measure the performance of the ARM core and FPGA block in handling streaming data by using the Ethernet traffic generator

### Complexity

Develop and measure an Ethernet-based product for 1 or 10G

**Keywords for this project**
- Ethernet
- System on Chip (SoC)
- VHDL

**Affinity**
- FPGA Development
- Software Development
- Ethernet knowledge

**Skills**
- Independent
- Competent in English
- Inquisitive

Are you a student with a can-do attitude and a passion for technology?
AimValley is your company!
**Why not join us today: students@aimvalley.com**



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