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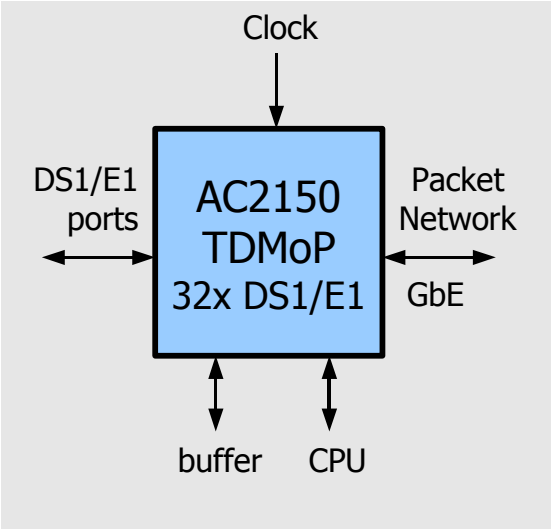
ADVANCE FACTSHEET

AC2150 - DS1/E1 TDM over Packet device



- **TDM over Packet solution for DS1/E1**
- **CESoPSN and SAToP TDM mappings**
- **Jitter and wander compliant to G.8261 and G.823/G.824**
- **Integrated framers and dual GbE ports**
- **Applications:**
  - **TDM over Packet CPE**
  - **TDM over Packet aggregation nodes**
  - **Wireless backhaul systems**
  - **Wireline network migration**

Overview

The AC2150 TDM over Packet device implements Circuit Emulation Services Interworking Functions (CES IWF) for 32 DS1/E1 TDM channels.

Each of the TDM ports may be asynchronously clocked on ingress and the reassembly function supports independent clock recovery for the TDM data on egress. Each channel operates in either adaptive and differential clock recovery mode.

The AC2150 implements the IETF and MEF8 defined SAToP and CESoPSN modes. These allow transport of either the full DS1/E1 channels, or bandwidth efficient fractional channels. The integrated DS1/E1 framers enable fault and performance monitoring, including test pattern insertion and loopback. The device supports Ethernet, VLAN and MPLS PWE3 packet headers and a dual Ethernet interface.

The device is ideally prepared for new protocols or standards evolution due to its FPGA based design.

Features

- TDM over Packet CES IWF for 32 DS1/E1 ports
- SAToP or CESoPSN transport mode selectable per channel (RFC4553 and RFC5086)
- SAToP: unstructured agnostic payload transport
- CESoPSN: transport of fractional DS1/E1
- Configurable amount of TDM data per packet
- Clock recovery mode selection per channel: adaptive or differential mode
- RTP header for differential clock: RFC3550
- RTP time stamp programmable at N * 8 kHz
- Jitter and wander compliant to ITU-T G.8261 and G.823 / G.824 for traffic interfaces
- Programmable initial and maximum jitter buffer, up to 32 ms per channel
- Packet resequencing and missing packet detection with TDM frame replication
- Integrated DS1/E1 framer provides alarm, fault and performance monitoring, and supports loopbacks and PRBS maintenance functionality
- Integrated Ethernet MAC enables flexible packet header processing of MAC addresses, VLAN tags and MPLS PWE3 headers

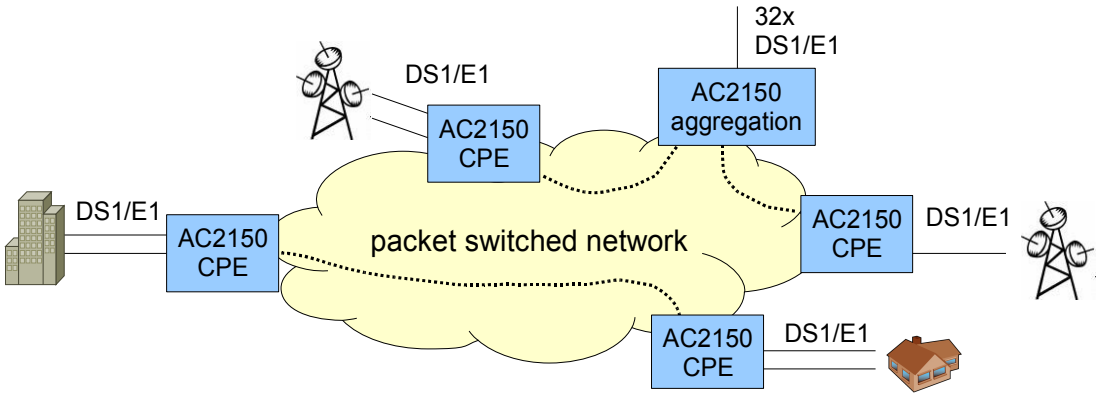
Interfaces

- TDM interface to LIU at 1.544 or 2.048 Mb/s
- Dual RGMII interface to PHY device
- Clock: 19.44 MHz
- ZBT SRAM buffer: 128k x 36
- 16-bit CPU interface

Technology and Package

- 65 nm CMOS technology
- 1.2V / 2.5V / 3.3V power supply
- 484-pin 23 x 23 mm FBGA package
- Typical power dissipation < 1.5 Watt

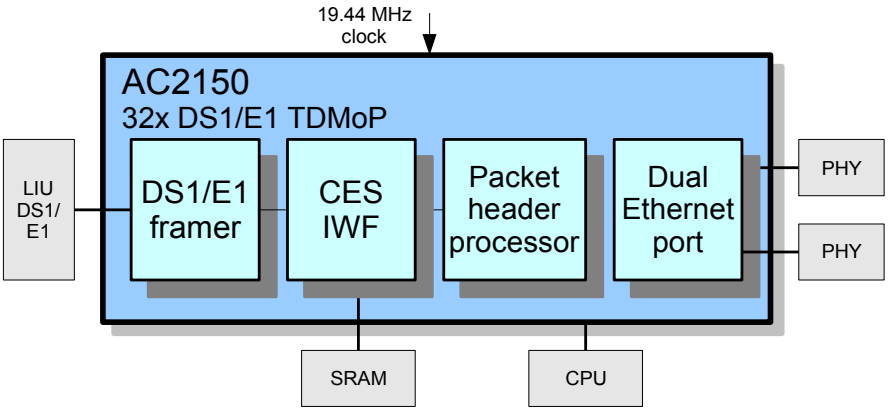
Applications and Block diagram



TDMoP CPE and aggregation applications

Typical system applications for the AC2150 include:

- TDMoP CPE and edge equipment
- Carrier Ethernet Switch or router blade for TDMoP network aggregation
- TDM business access equipment for leased line migration
- RBS or BTS base station network cards
- CMTS cable headend
- AMC I/O cards for ATCA and MicroTCA



Device block diagram and interfaces

A companion device, the AC2380 - OC12/STM4 TDMoP Gateway, targets TDM over Packet aggregation applications. The AC2150 and AC2380 are based on the same processing core and allow for seamless end-to-end interworking.

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